WHAT IS CLAIMED IS:

1. A plasma display panel driving circuit for generating a ramp pulse for linearly increasing or decreasing a panel capacitor voltage of a plasma display panel, comprising:

a transistor in which at least one parasitic capacitance is formed;

a negative feedback element coupled to the transistor, for performing negative feedback control on a voltage charged in the parasitic capacitance so that the transistor may operate as a constant current source; and

a first capacitor coupled between a gate and an active node of the transistor, the first capacitor having a temperature characteristic opposite to a temperature characteristic of the negative feedback element.

2. The plasma display panel driving circuit of claim 1, wherein the first capacitor is coupled between the gate and a drain of the transistor, and

the negative feedback element comprises a second capacitor, coupled in parallel with the first capacitor, between the gate and the drain of the transistor.

3. The plasma display panel driving circuit of claim 2, further comprising a third capacitor coupled between the gate and a source of the transistor, the third capacitor having a temperature characteristic opposite to a temperature characteristic of the parasitic capacitance formed between the gate and the source of the transistor.

4. The plasma display panel driving circuit of claim 2, further comprising a third capacitor coupled between the gate and the drain of the transistor, the third capacitor having a

temperature characteristic to opposite that of a temperature characteristic of the parasitic capacitance formed between the gate and the drain of the transistor.

5. The plasma display panel driving circuit of claim 1, wherein the negative feedback element comprises a resistor coupled to an output end of the transistor, and the first capacitor is coupled between the output end of the transistor and the gate of the transistor.

6. The plasma display panel driving circuit of claim 2, further comprising a third transistor coupled in parallel to the parasitic capacitance of the transistor, and having a temperature characteristic opposite to a temperature characteristic of the parasitic capacitance.

7. A plasma display panel driving circuit for generating a ramp pulse for linearly increasing or decreasing a panel capacitor voltage of a plasma display panel, comprising:

a transistor having parasitic capacitance formed between a gate and a source thereof;

a first capacitor coupled between the gate and a drain of the transistor; and

a second capacitor coupled between the gate and the drain of the transistor, the second capacitor having a temperature characteristic opposite a temperature characteristic of the first transistor.

8. The plasma display panel driving circuit of claim 7, further comprising a third capacitor coupled between the gate and a source of the transistor, the third capacitor having a temperature characteristic opposite to a temperature characteristic of the parasitic capacitance.

9. A plasma display panel driving circuit for generating a ramp pulse for linearly increasing or decreasing a panel capacitor voltage of a plasma display panel, comprising:

a transistor having a parasitic capacitance formed between a gate and a source thereof; and

a first capacitor coupled between the gate and the source of the transistor, the first capacitor having a temperature characteristic opposite to a temperature characteristic of the parasitic capacitance.

10. The plasma display panel driving circuit of claim 9, further comprising a second capacitor coupled between the gate and a drain of the transistor.

11. The plasma display panel driving circuit of claim 10, further comprising a third capacitor coupled between the gate and the drain node of the transistor, the third capacitor having a temperature characteristic opposite to a temperature characteristic of the second transistor.

12. The plasma display panel driving circuit of claim 10, further comprising a resistor coupled to the source of the transistor.